What is claimed is:

[Claim 1] A power reduction circuit, comprising:

a logic block; and
at least one micro-electromechanical (MEM) switch for selectively disabling the logic block.

[Claim 2] The power reduction circuit of claim 1, wherein the logic block is selected from the group consisting of latches, memory arrays, embedded memory arrays, control logic, registers, application specific integrated circuit (ASIC) cores, microprocessors, and multithreaded processors.

[Claim 3] The power reduction circuit of claim 2, wherein the latch comprises a level-sensitive scan design (LSSD) latch.

[Claim 4] The power reduction circuit of claim 1, wherein the at least one MEM switch for selectively disabling the logic block further comprises:

a MEM switch for selectively disconnecting the logic block from power; and
a MEM switch for selectively disconnecting the logic block from ground.

[Claim 5] The power reduction circuit of claim 1, further comprising:

a bypass line connected between an input and output of the logic block; and
a MEM switch for selectively disconnecting the bypass line.

[Claim 6] The power reduction system of claim 1, further comprising:

a MEM switch for selectively disconnecting an output of the logic block.

[Claim 7] The power reduction system of claim 1, further comprising:

a MEM switch for selectively disconnecting an input of the logic block.

[Claim 8] A method for power reduction, comprising:

providing a logic block; and
selectively disabling the logic block using at least one micro-electromechanical (MEM) switch.

[Claim 9] The method of claim 8, wherein the logic block is selected from the group consisting of latches, memory arrays, embedded memory arrays, control logic, registers, application specific integrated circuit (ASIC) cores, microprocessors, and multithreaded processors.

[Claim 10] The method of claim 8, wherein the latch comprises a level-sensitive scan design (LSSD) latch.

[Claim 11] The method of claim 8, wherein the step of selectively disabling the logic block further comprises:

selectively disconnecting the logic block from power using a MEM switch; and selectively disconnecting the logic block from ground using a MEM switch.

[Claim 12] The method of claim 8, further comprising:

providing a bypass line between an input and output of the logic block; and selectively disconnecting the bypass line using a MEM switch.

[Claim 13] The method of claim 8, further comprising:

selectively disconnecting an output of the logic block using a MEM switch.

[Claim 14] The method of claim 8, further comprising:

selectively disconnecting an input of the logic block using a MEM switch.

[Claim 15] A circuit, comprising:

a logic block;
a micro-electromechanical (MEM) switch for selectively disconnecting the logic block from power;
a MEM switch for selectively disconnecting the logic block from ground;
a bypass line connected between an input and output of the logic block for passing data around the logic block; and
a MEM switch for selectively disconnecting the bypass line.

[Claim 16] The circuit of claim 15, wherein the logic block is selected from the group consisting of latches, memory arrays, embedded memory arrays, control logic, registers, application specific integrated circuit (ASIC) cores, microprocessors, and multithreaded processors.

[Claim 17] The circuit of claim 15, further comprising:

a MEM switch for selectively disconnecting an output of the logic block to prevent data from appearing on the output of the logic block.

[Claim 18] The circuit of claim 15, further comprising:

a MEM switch for selectively disconnecting the input of the logic block to separate the input of the logic block from preceding circuitry.

[Claim 19] The circuit of claim 15, wherein, in an operational mode of the logic block, the MEM switch for selectively disconnecting the logic block from power and the MEM switch for selectively disconnecting the logic block from ground are closed to provide the logic block with power, and the MEM switch for selectively disconnecting the bypass line is open to prevent data from passing around the logic block.

[Claim 20] The circuit of claim 15, wherein, in a non-operational mode of the logic block, the MEM switch for selectively disconnecting the logic block from power and the MEM switch for selectively disconnecting the logic block from ground are open, thereby disconnecting the logic block from power, and the MEM switch for selectively disconnecting the bypass line is closed, thereby allowing data to pass around the logic block.